AF/2143

#14
T.D.
03/26/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No.: **JA9-98-196**

In re Application of: §

TADOKORO ET AL. §

Examiner: **DELGADO, M.**

Serial No.: **09/510,569** §

Art Unit: **2143**

Filed: **22 FEBRUARY 2000** §

For: **HARDWARE SETUP METHOD** §

REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated July 16, 2003.

CERTIFICATE OF MAILING
37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as First-Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date below.

August 1, 2003
Date

Signature

REMARKS

Claim 1 (and similarly Claims 5 and 17) recites a step of "storing a hardware setup program and a plurality of dynamic link modules in a server data processing system." On page 8 of the Examiner's Answer, the Examiner asserts that the claimed storing step is disclosed by *Rakavy* in col. 10, lines 55-60. The Examiner further explains that "it is inherent that the code and data (hardware setup program and dynamic link modules) had to be stored in advance on the workstation (server data processing system) for this [loader service] operation to be possible."

However, the Examiner's interpretation of the claimed hardware setup program is not consistent with its usage as recited in the remaining of Claim 1. This is because Claim 1 also recites a step of "modifying hardware configuration data within said data processing system according to instructions generated from said execution of said hardware setup program within said server data processing system." In other words, instructions are initially generated within the server data processing system via an execution of the above-mentioned hardware setup program within the server data processing system, and the instructions generated within the server data processing system are then utilized to modify the hardware configuration data within the data processing system. Thus, the operations performed by the claimed hardware setup program are different from *Rakavy*'s loader service.

In addition, on page 10 of the Examiner's Answer, the Examiner asserts the claimed modifying step is disclosed by *Rakavy* in col. 4, lines 30-35. According to col. 4, lines 30-35, *Rakavy* states:

> A second computer coupled to the first computer through the network may transfer commands, status and data prior to the loading of the operating system or after operating system failure. The first computer may be further provided with a means for alerting the second computer in the event of a POST failure or operating system crash.

As shown, *Rakavy* discloses a second computer (*i.e.*, the claimed data processing system) transfers commands, status and data to a first computer (*i.e.*, the claimed server data processing system). Thus, it is clear that *Rakavy* does not teach or suggest "modifying hardware configuration data

within said data processing system according to instructions generated from ... said server data processing system," as claimed because the above-mentioned hardware setup program was not mentioned in col. 4, lines 30-35. Also, if the above-mentioned hardware setup program is intended for providing a loader service, as interpreted by the Examiner on page 8, the same hardware setup program cannot be used for fault recovery, as interpreted by the Examiner on page 10. Since the claimed invention recites novel features that are not taught or suggested by *Rakavy*, the § 102 rejection is improper.

On page 9 of the Examiner's Answer, the Examiner asserts that the claimed de-coupling step is disclosed in col. 11, lines 1-30 of *Rakavy* as "removing the electronic connection (decoupling) from computer (400) after a successful hardware setup is completed." The term "coupling" generally means being joined together, and the term "de-coupling" generally means being separated apart. In the context of Claim 1, the recited step of "de-coupling said data processing system from said server data processing system" means that the data processing system is being separated apart from the server data processing system. Also, according to col. 11, lines 1-30, *Rakavy* states:

> All the threads described above continue to run throughout the time when the network enhanced BIOS **600** is active, generally until the POST completes. As noted above, in the case when there is no intervention from the management workstation **200**, and there is no POST error, an alert indicating that the POST is successfully completed is sent **431**.
>
> The network enhanced BIOS **600** may further install its own interrupt handlers for the timer tick interrupt (interrupt 08H on 80x86 microprocessors). The timer tick interrupt vector is directed to a procedure implementing step **860** in FIG. **8**, which forces the current real mode code to save its state and jump to the network enhanced BIOS **600**. This enables the network enhanced BIOS **600** to continue to obtain CPU control at regular intervals while certain real-mode operating systems, such as MS-DOS, load and are running. Note that the BIOS screen display interrupt 10H may have previously been redirected to a handler as part of the remote console facility already described, and this mechanism remains in place. CPU control then passes to the bootstrap **432**.
>
> If the operating system to be loaded is a protected mode operating system, such as NetWare or Windows-NT, then it will switch the processor to protected mode, replace the interrupt vectors including the timer tick and screen display interrupts described above, take over control of the CPU **110**, and except for its crash recovery functions, the network enhanced BIOS will cease to function.
>
> If a real mode operating system such as MS-DOS without any protected mode memory manager is loaded then the network enhanced BIOS code will remain in extended memory.

Thus, it is clear from the above-stated paragraph that *Rakavy* does not teach or suggest the claimed de-coupling step in col. 11, lines 1-30 because computer **400** was not being separated from workstation **200**. In fact, computer **400** was not even mentioned in the above-stated paragraph at all. Since the claimed invention recites novel features that are not taught or suggested by *Rakavy*, the § 102 rejection is improper.

For the reasons stated above, Appellants believe the § 102 rejection for Claims 1-8 and 17-20 is improper and should be reversed.

No fee or extension of time is believed to be necessary; however, in the event that any fee or extension of time is required for the prosecution of this application, please charge that fee or extension of time requested to the Bracewell & Patterson Deposit Account **50-0259**.

Respectfully submitted,

Antony P. Ng
Registration No. 43,427
BRACEWELL & PATTERSON, LLP
111 Congress Avenue, Suite 2300
Austin, Texas 78701
512.542.2134

ATTORNEY FOR APPELLANTS